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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,348	08/06/2003	George Ernest Harris	TI-35894	8892

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2117	

NOTIFICATION DATE	DELIVERY MODE
09/21/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/635,348	HARRIS ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *16-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on 3/13/2007, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

JACQUES LOUIS-JACQUES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Priority

Acknowledgment is made that no priority is claimed for this application and as such the filing date, 8/6/2003, is being used for this examination.

Information Disclosure Statement

Acknowledgment is made that an IDS has not been provided with the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification lacks enablement with respect to the claimed "layout parasitics." The specification describes on page 3 lines 18-23 only that "the test structure contains a dummy match row unit coupled to the memory array and configured to match layout parasitics of the match lines of the memory cells, ...". It is unclear from reading the specification how to "match layout parasitics of the match lines." For the purposes of examination the dummy mach row unit and the dummy match column unit are considered as equivocates to each other.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1 and 15, it is unclear to the examiner how one skill in the art can configure a dummy match row "to match layout parasitics of match lines," since a match lines is a wire or line and the dummy match row is circuitry constructed for the purpose of outputting an electrical signal.

Claims 2-14 are dependent on claim 1 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered on their merits.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes et al. (US 6691252) and Giles et al. (US 4680760).

2. As per claim 1: Both Hughes and Giles teach an electronic memory test structure for testing a CAM having a memory array containing memory cells, the electronic test structure comprising:

Hughes teaches the electronic memory test structure comprising:

Column testing of a CAM memory array (column 6 lines 8-9);

Row testing of a CAM memory array (column 7 lines 2-4);

A timing circuit coupled to both the columns and row (column 9 lines 59-65).

A control circuit coupled to the timing circuit (column 9 lines 59-65).

Hughes does not teach a column or row dummy match unit coupled to the memory array.

Giles teaches the electronic memory test structure comprising:

A dummy match row unit (column 2 line 37, 28; figure 2) coupled to the memory array (10- CAM array; figure 1) through the match lines (18-match lines; figure 2), said dummy match row unit (28; figure 2) being configured so as to match bitline loading (20 and 22; figure 1 and 2) of the memory cells during a search.

However those of ordinary skill in the art would recognize that rotating Giles' test structure would result in the dummy match row (column 2 lines 20-22, 37-39) being a dummy match column unit.

Therefore one of ordinary skill in the art would be motivated to rotate Giles' test structure to obtain a dummy match column unit in order to perform vertical testing of a CAM array to isolate and test individual CAM array cells in a row. Furthermore, one would be motivated to combine Hughes' column and row testing structure with Giles' dummy match unit structure for testing a CAM having a memory array according to Giles, test each component of the test structure (column 2 lines 53-55), and according to Hughes, capitalize on chip surface area "real estate" (column 1 lines 32-33).

3. As per claim 2: Giles teaches the above electronic memory test structure wherein the dummy match row (column 2 lines 20-22, 37-39) is configured so as not to pull the match lines (18; figure 2) to the logic high state during a normal search mode (column 2 lines 36-39).

4. As per claim 3: Hughes teaches the above electronic memory test structure wherein the control circuit (column 9 line 62) causes a transition so as to match timing of the bitline transitions of the memory cells (column 3 lines 55-59).

5. As per claim 4: Giles teaches the above electronic memory test structure wherein a dummy timing circuit (column 5 lines 13-16) always generates a miss on the dummy match line (column 2 lines 36-39).

Giles does not teach a miss on the dummy match line (18-match; figure 2) caused by a transit of the dummy match line (18-match; figure 2) to a high (1) state.

However it would have been obvious to one of ordinary skill in the art at the time the invention was made to invert the miss taught by Giles, indicated by a zero (0) into a high state (1), since it was well known in the art to invert a signal to get the desired value ((1) to indicate a miss) based on the logic of the circuit.

Therefore one would be motivated to invert Giles's logic where when doing so the cost of circuitry to implement the inverted logic is more reliable or cost effective.

6. As per claim 5: Giles teaches the above electronic memory test structure wherein a dummy match control circuit (28; figure 2) has a low search input and one of a low match state and a high match state (column 2 lines 29-39); and mask inputs are

set to high so that the memory array (10; figure 1) is not searched (column 2 lines 53-55).

7. As per claim 6: Hughes teaches the above electronic memory test structure wherein a priority encoder is coupled to the memory array through the match lines (column 9 lines 39-45).

8. As per claim 7: Hughes teaches the above electronic memory test structure wherein a priority encoder control unit is coupled to the priority encoder, and to the dummy match row unit through the dummy match line (column 9 line 59-65, figure 7, column 9 line 44-46).

9. As per claim 8: Hughes teaches the above electronic memory test structure wherein each cell of a match column generating a logic high level on the match lines during a test mode for passing onto the memory array (column 6 lines 5-13, figure 2).

10. As per claim 9: Giles teaches the above electronic memory test structure wherein any cell of the dummy match row does not generate a logic high level on the match lines during another test mode (column 4 lines 9-17).

11. As per claim 10: Hughes teaches the above electronic memory test structure wherein the priority encoder receives all the generated logic high levels through the match lines (column 9 lines 39-45, figure 7).

12. As per claim 11: Giles teaches the above electronic memory test structure wherein the match lines (18; figure 2) from the memory array (10; figure 1) to the priority encoder (32; figure 1) are at low levels (column 2 line 36-39).

13. As per claim 12: Giles teaches the above electronic memory test structure wherein the test mode is all-hits mode (column 4 lines 9-13).

14. As per claim 13: Giles teaches the above electronic memory test structure wherein the other test mode is all hits (column 4 lines 9-21).

Giles does not teach the other test mode is all-misses mode.

However It would have been obvious to one of ordinary skill in the art at the time the invention was made to invert the all hit test (column 4 lines 15-21) taught by Giles.

Therefore one would be motivated to do so since it was well known in the art as indicated by Hughes that single cells may become stuck at a value regardless of the data attempted to be written into them (column 2 lines 4-16).

15. As per claim 14: Giles teaches the above electronic memory test structure wherein the electronic memory test structure further comprise:

A dummy read column unit (34-entry selection; figure 1) coupled to the memory array (10-CAM array; figure 1) for matching timing (entry selection control; figure 1) characteristics of the wordline signals (column 3 lines 37-38, column 4 lines 11-21) of the memory array (10-CAM array; figure 1).

Giles does not directly teach a dummy read row unit for matching timing characteristics of the wordline signals of the memory array.

Hughes teaches an interconnected match latch unit (707; figure 7) and wordline driver (706; figure 7) coupled between the priority encoder (705- redundancy allocation circuitry) and memory array (701-CAM; figure 7).

However It would have been obvious to one of ordinary skill in the art at the time the invention was made to rotate Giles' CAM memory array so that the dummy read column unit (34- entry selection; figure 1) becomes a dummy read row unit.

Therefore one would be motivated to perform this rotation to implement row testing to isolate and test individual CAM array cells in a row as stated above as per claim 1.

16. As per claim 15: Giles teaches an integrated circuit for testing a CAM having a memory array containing memory cells (10-CAM array; figure 1), comprising:

An integrated circuit substrate having a dummy match row unit (28; figure 2, column 2 lines 32, 37-39, figure 1) coupled to the memory array (10-CAM array; figure 1), said dummy match row unit (28; figure 2) configured to match layout parasitics of the match lines of the memory cells (column 2 lines 27-39);

A dummy timing circuit coupled to the dummy match row (system clock; column 5 lines 15-16), said dummy timing circuit being configured to always generate a miss on a dummy match line during the search (column 2 lines 37-39); and

Giles does not directly teach:

A dummy match column (vertical set of 28; figure 2) having dummy match cells (28; figure 2) coupled to the memory array through the match lines (Match; figure 1), said dummy match column (vertical set of 28; figure 2) being configured so as to match bitline loading of the memory cells during a search (20 and 22; figure 1 and 2). However it would have been obvious to one of ordinary skill in the art at the time the invention

was made to rotate Giles' CAM memory array so that the dummy match column unit (34- entry selection; figure 1) becomes the claimed dummy read row unit. One would be motivated to perform this rotation to implement row testing to isolate and test individual CAM array cells in a row as stated above as per claim 1.

A dummy timing circuit (system clock; column 5 lines 15-16) coupled to the dummy match column and to the dummy match row, said dummy timing circuit being configured to always generate a miss on a dummy match line during the search (column 2 lines 37-39). However it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the timing circuit (system clock; column 5 lines 15-16) coupled to both the dummy match row and column and to always generate a miss on a dummy match line. One would be motivated to couple both the dummy row and column to the time circuit for synchronization and to generate a miss on a dummy match line to reset or set a default setting on the match line.

A dummy match control circuit coupled to the dummy timing circuit. However Hughes teaches in an analogous art a control circuit and a CPU (column 9 line 62). Therefore since all electronic components in a working electronic system require a connection to a CPU or control unit/circuit it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Hughes' control circuit coupled to the dummy timing circuit. One would be motivated to have a control circuit coupled to the dummy timing circuit since it is a necessity for a working electronic system.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. Riedlinger (U.S. Patent 6539466 B1), discloses both a dummy Row and Column within a CAM

ii. Huang (U.S. Patent 6999331 B2), discloses Dummy Cam Cells within a CAM array, wherein corresponding rows within the CAM can be enabled or disabled for comparison with input data, thereby reducing processing time.

iii. Yetter (U.S. Patent 5289403), discloses both a Dummy Column and a Dummy Row in conjunction with a CAM memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

9/12/07
JAMES C. KERVEROS
PRIMARY EXAMINER

Steven D. Radosevich
Examiner
Art Unit 2117